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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,970	09/28/2001	Jeffrey D. Harper	033257/236160	5811

55207 7590 03/11/2008

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
03/11/2008	PAPER

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY D. HARPER

Appeal 2007-3324
Application 09/966,970
Technology Center 2600

Decided: March 11, 2008

Before: KENNETH W. HAIRSTON, ROBERT E. NAPPI, and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 (2002) from a final rejection of claims 1-3, 5-10, 12, 14-16, 18-20, 23-25, and 27-52. We have jurisdiction under 35 U.S.C. § 6(b) (2002).

Appellant discloses a method for processing image data which employs dual capture buffers. The buffers provide simultaneous image capture and image display processing.

The representative claim under appeal reads as follows:

1. An imaging device for simultaneous image capture and image display updating, the device comprising:

an imager for capturing image data;

a central processing unit (CPU) in communication with the imager and issues commands to capture image data;

a direct memory access module in communication with the imager and the CPU;

a first image capture buffer, accessible to the CPU, that temporarily stores first-in-time captured image data prior to displaying first-in-time image data:

a second image capture buffer, accessible to the CPU, that temporarily stores second-in-time captured image data prior to displaying second-in-time image data; and

an image enhancer for enhancing image data stored in the first and second image capture buffers prior to display.

Appealed Rejections

The Examiner rejected claims 1-3, 5-10, 12, 14-16, 18-20, 23-25, and 27-52 under 35 U.S.C. § 103(a) (2004) based on the collective teachings of Appellant's admitted prior art and Rao.

The References

The prior art relied upon by the Examiner in rejecting the claims on appeal is:[1]

Rao	WO 97/06523	Feb. 20, 1997

[1] The Examiner also relied on Appellant's admitted prior art (Ans. 3-5).

Appellant contends that the Examiner failed to present a prima facie case of obviousness because there is insufficient motivation to combine Appellants' admitted prior art (*hereinafter* APA) and Rao (Br. 6). Appellant has not separately argued the rejected claims; thus we group all of the rejected claims together. We take claim 1 as representative of the claims on appeal. See 35 C.F.R. 41.37(c)(1)(vii).

We *affirm*.

ISSUE

The issue is whether the Examiner erred in his finding that the collective teachings of the APA and Rao render obvious the claim limitations of first and second image capture buffers.

FINDINGS OF FACT

1. As background, Appellant states:

> Portable imaging devices such as bar code readers, optical character readers, digital cameras and the like have come into widespread use in large numbers of retail, industrial and medical applications. Such imaging devices are used to perform routine data entry functions such as pricing, inventory control, etc., with an accuracy and reliability that far exceeds that of manual data entry. These and other advantages, such as high data throughput rates and direct compatibility with data processing devices and systems, assures that imaging devices will become more prevalent in the future. As the use of such devices increases the demands on the devices will increase as well. These demands will dictate that the portable imaging devices of the future read, record and decode ever-increasing quantities and densities of optically encoded data.
>
> …[C]urrent imaging devices are limited by image update rates that may require the user to move or re-position the imager, wait for a

> display and incur a frustrating delay. If that delay is long enough there is a tendency on the part of the user to overshoot; the user continues to move the device with the aspiration of obtaining the desired image on the display when in fact the desired image has already passed.
>
> In accordance with the prior art, Fig. 1 is a simplified block diagram of portable imaging device hardware and software modules….The imager 20 captures images and the DMA module stores the image in memory module 60. An image capture buffer 70 within the memory module stores the image data prior to displaying the image on a display, such as liquid crystal display (LCD) 80.
>
> As shown in the timeline of Fig. 2, a typical imaging device will capture 30 frames per second or one frame every 33 milliseconds. This is commonly referred to as the image capture cycle (i.e. the time required for the imager to expose the image and ship the data to memory). In the timeline of Fig. 2, the image capture cycle is 33 milliseconds, meaning that once every 33 milliseconds the imager exposes a new frame and sends this image to memory. In prior art imaging devices if a command to capture an image is issued while the imager is in the middle of displaying an image, the next image capture routine will commence once a new image capture cycle begins.

(Spec. 1: 13 to Spec. 2:24).

2. Appellant states that due to the time (about 10 to 20 milliseconds) required to pre-process (i.e. reformat and enhance the image) and then "paint" the image on the display after it has been captured, the imager cannot capture all the desired frames. That is, due to the pre-processing, the device cannot capture another desired image while the device is writing data to the display screen. (Spec. 3). Appellant states: "This results in only about 15 frames per second being painted on the display during the aiming routine." (Spec. 4: 1-2). Due to the processing delay,

> a need exists to develop an imaging device that will improve the speed at which images are updated on the imaging device displays. In this regard, such a device will provide the capability to display every frame that the image is capable of capturing.

(Spec. 4: 3-5).

3. Rao describes a processing system having a plurality of frame buffer areas (110/110). A central processing unit is "operable to update display data in a first selected one from the frame buffer areas (110/111) while display data from a second selected one of the frame buffer areas (110/111) provides data for refresh of a display screen of an associated display device." (Abstract).

PRINCIPLES OF LAW

On appeal, Appellant bears the burden of showing that the Examiner erred. Appellant may sustain this burden by showing that, where the Examiner relies on a combination of disclosures, the Examiner failed to provide sufficient evidence to show that one having ordinary skill in the art would have done what Appellant did. *United States v. Adams*, 383 U.S. 39, 47 (1966); *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick, Co.*, 464 F.3d 1356, 1360-61 (Fed. Cir. 2006).

Appellant may also show that the Examiner has failed to meet his initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden

shifts to the Appellant to overcome the prima facie case with argument and/or evidence. *See Id.*

The Examiner's articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d at 988.

"[W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *KSR Int'l Co. v. Teleflex Inc.,* 127 S. Ct. 1727, 1740 (2007).

> For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* and *Anderson's-Black Rock* are illustrative – a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id.

It is well settled that the prior art relevant to an obviousness determination encompasses not only the field of the inventor's endeavor but also any analogous arts. *Heidelberger Druckmaschinen AG v. Hantscho Commercial Products Inc.*, 21 F.3d 1068, 1071 (Fed. Cir. 1994). The test of whether a reference is from a nonanalogous art is first, whether it is within the field of the inventor's endeavor, and second, if it is not, whether it is reasonably pertinent to the particular problem with which the inventor was involved. *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979). A reference is reasonably pertinent if, even though it may be in a different field of endeavor, it is one which because of the matter with which it deals, logically

would have commended itself to an inventor's attention in considering his problem. *In re Clay*, 966 F.2d 656, 659 (Fed. Cir. 1992).

ANALYSIS

The Examiner found that Appellant's APA taught all of the claimed features except for the second buffer required by claim 1. The Examiner further found that Rao teaches the second buffer (Ans. 3). Appellant does not dispute the Examiner's findings just described, but argues that Rao is not analogous to the claimed subject matter (Br. 7), and alternatively, even if Rao were analogous art, the Examiner has not cited any teaching or suggestion required to combine Rao with the APA (Br. 8). We adopt the Examiner's undisputed findings as our own as supported by the record (*see* Ans. 3-5, FF 1).

We turn first to the argument that Rao is not analogous art. We concur with the Examiner's finding that Rao is analogous art. (Ans. 4). The test of whether a reference is from a nonanalogous art is first, whether it is within the field of the inventor's endeavor, and second, if it is not, whether it is reasonably pertinent to the particular problem with which the inventor was involved. *In re Wood*, 599 F.2d at 1036.

We determine that Rao meets both prongs of the test. We have little trouble finding that Appellant's field of endeavor relates to the general field of computer data processing (FF 1, 2). "While computer technology is an exploding one, '(i)t is but an even handed application to require that those persons granted the benefit of a patent monopoly be charged with an

awareness' of that technology." *Dann v. Johnston*, 96 S.Ct. 1393, 1398 (1976) (quoting *Graham v. Deere Co.*, 86 S.Ct. 684, 695 (1966), and holding that a patent to analyze data processing in a non-banking context rendered obvious a similar invention directed to banking). Appellant's argument that Rao's data processing disclosure is not available prior art because Appellant's invention is limited to an imaging computer system (Br. 7) is analogous to the argument dismissed in *Dann*. As *Dann* makes clear, the grant of a monopoly requires Appellant to be charged with the awareness of data processing knowledge that is not limited to imaging systems just as the respondent's knowledge in *Dann* could not be limited to banking industry systems.[2]

Further, Appellant acknowledges that the disclosed invention focuses on data processing, to wit:

> In an imaging device, the ability to paint the frames to a screen is first dictated by the ability to the imager to deliver said frames and secondly by the *ability to process these frames* and make them available for painting. The present invention focuses on the second portion by providing multiple buffers and methods of user [sic] therefore.

(Br. 8) (emphasis supplied).

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[2] Even if either the pertinent prior art or field of endeavor were limited to imaging systems as Appellant argues, Appellant does not challenge the Examiner's finding that it would have been well known to employ image readers like scanners or cameras with computers such as Rao's (Ans. 4). In other words, Rao's teachings apply to scanning computer systems. The Examiner's finding is supported by Appellant's statement in the "Background of the Invention" section that "direct compatibility with data processing devices and systems[,] assures that imaging devices will become more prevalent in the future" (Spec. 1: 18-19).

> Likewise, Rao states:
>
> [T]he need has arisen for improved apparatus, systems, and methods for more efficiently constructing and managing memory *in processing and display systems*. In particular, the need has arisen for techniques to conserve CPU operating cycles during display updates. Advantageously, such techniques would free the CPU to perform other critical operations and thus improve overall system performance.

Rao (4: 32 to 5: 4) (emphasis supplied).

Hence, both Rao and Appellant are concerned in general with processing data in computer systems, satisfying the first prong of the *In re Wood* test. We turn next to the second prong of the test.

We also find that Rao satisfies the second prong. That is, we find that both Rao and Appellant are concerned with a particular problem of inefficient prior art memory systems involved in moving data from a single buffer to a display screen during "refresh" (Rao, 14: 18) or "painting" (Spec. 10: 16) operations.

In particular, Appellant describes a shortcoming of an APA imager otherwise able to capture 30 frames per second as being due to limitations in APA single buffer processing systems resulting in a display of only 15 frames per second – due to processing time absorbed in the APA memory 60 and buffer 70 prior to "painting" the image on the display 80 (FF 1, 2; Spec. Fig. 1; 3: 19 to 4: 2). Appellant explains: "Therefore, a need exists to develop an imaging device that will improve the speed at which images are updated on imaging device displays." (Spec. 4: 3-4).

Appellant's solution to the overall slow processing speed is to employ two buffers to replace the APA single buffer, resulting in an efficient

transfer of data to one buffer with a simultaneous transfer of data from the other buffer to the display. (Spec. 5: 18-24). In short, as Appellant notes, a two buffer solution renders a more efficient system (Spec. 4: 20-21).

Similarly, Rao also solves an inefficiency problem associated with prior art single buffer display systems by employing a system that is the same as or similar to Appellant's two buffer solution (Rao, 13: 12 to 15: 16). In Rao's system, like Appellant's system, data is transferred from one buffer to the display and from memory to the other buffer simultaneously (*id.*, FF 2-3). Efficiency increases over the single buffer prior art systems in part because "the number of CPU clock cycles which are required to perform the screen update is essentially halved" (Rao 15: 5-7).[3]

Thus, Rao's teaching implies that prior art single buffer systems are too slow by at least a factor of two, while Appellant discloses precisely the same problem with prior art single buffer display systems; i.e., they are also disclosed as too slow by at least a factor of two - because the prior art single buffer system can only process 15 of the 30 frames that the imager can otherwise capture (FF 1, 2).[4] Consequently, we are not persuaded by

[3] Rao's system also gains efficiency in the refresh cycle: "Since 75% of all display processing time is normally used for screen refresh, the ability to shift the display refresh to the display controller can substantially improve system performance as the CPU 101 is made available for other tasks." (Rao, 14: 18-21).

[4] Appellant states that prior art imaging systems are unable to capture an image until the display routine is finished. (Br. 5, Spec. 3: 13-18). The prior art system's inability to perform simultaneous capture and display cycles is due to the single buffer employed in those systems. Rao also recognizes that inefficiency occurs because the two cycles (refresh and display) cannot be performed simultaneously in prior art single buffer systems (6:29 to 7:12; 13:12 to 15:16). To overcome the inefficiency, Rao's display update and screen refresh cycles respectively perform the same functions as Appellant's

Appellant's arguments that Rao does not address "lag," or "timing," or otherwise suggest an increase in the refresh rate (Br. 8, 9).

In essence, as indicated above, prior art single buffer systems are inefficient because they are unable to process capture and refresh cycles concurrently (*see* FF 2, n. 4 *supra*). In other words, the inefficiency is based upon the data becoming bottlenecked in the prior art single buffers prior to display. While Rao describes the problem in terms of the CPU's inability to perform refresh and display quickly (i.e., too much CPU time is allocated to transferring data to and from the single buffer system, *see* nn. 3-4 *supra*), the data involved in Rao's described prior art systems is also bottlenecked in the single buffer because the CPU simply cannot move it to and fro quickly enough. Therefore, Appellant and Rao each provide the same solution to the same problem of inefficiency associated with bottlenecked data in single buffer/display systems – a two buffer memory/display system.

Given the nature of the Appellant's problem of bottlenecked data in a single buffer system, one of ordinary skill in the art would have consulted prior art areas to include Rao's teaching of employing more than one buffer to reduce processing time and increase efficiency associated with similar prior art single buffer systems. *See, e.g., In re Heldt*, 433 F.2d 808, 812 (CCPA 1970), *In re Ellis*, 476 F.2d 1370, 1372 (CCPA 1973), *Union Carbide Corp. v. American Can Co.*, 724 F.2d 1567, 1572 (Fed. Cir. 1984); *In re GPAC Inc.*, 57 F.3d 1573, 1578-79 (Fed. Cir. 1995). This being the

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capture and refresh cycles (i.e., "new" data is transferred to the display update or capture buffer at the same time "old" data or refresh data is transferred from another buffer to the display screen). The Examiner recognized that Appellant and Rao address the same or similar problem in the same manner (*see* n. 5 below).

case, the second prong of the test in *Wood* is satisfied and Rao is analogous art.

In sum, we find that Appellant's and Rao's disclosures either involve the same field of endeavor of computer processing systems or a solution to the same particular problem of inefficient computer memory/display systems. Both Appellant and Rao solve the particular problem by employing the same solution – the use of two buffers.

Consequently, we do not consider either the pertinent prior art or field of endeavor to be limited to imaging devices even if the claims are.

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.
>
> ....
>
> ...Under the correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed in the patent [or application] can provide a reason for combining the elements in the manner claimed.

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1740, 1742 (2007). *See also Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563, 1580 (Fed. Cir. 1983)(scope of pertinent prior art not limited to pacemakers but also includes electronics involving battery voltage sensing).

We turn to Appellant's final argument that there is no suggestion or motivation to combine Rao with the APA. The analogous art "test begins the inquiry into whether a skilled artisan would have been motivated to combine references." *In re Kahn*, 441 F.3d at 987. The Examiner's determination, with which we concur, that Rao provides the same or similar solution to the same or similar problem as Appellant, supports the

Examiner's use of Rao in the obviousness rejection and indicates a motivation for one of ordinary skill to consult the reference.[5] *Id.* n. 3.

Moreover, "when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *KSR Int'l Co. v. Teleflex Inc.,* 127 S. Ct. at 1740. The dual buffer structure of Rao was known in the art. Appellant merely altered the prior art single buffer by replacing it with a dual buffer system as taught by Rao. No more than the predictable result of increasing the efficiency and speed of the computer system occurred as indicated above.

Consequently, because the result would have rendered a predictable efficiency gain as implied by the Examiner's finding that double buffering provides concurrent update and refresh, and given the known market demands to increase computer processing speeds coupled with the known prior art problem associated with inefficient single buffer/display systems, we determine the Examiner's obviousness determination to be legally sufficient.

CONCLUSION

Appellant failed to meet the burden of asserting error in the Examiner's rejection. *See Adams*, 383 U.S. at 47; *In re Kahn*, 441 F.3d at 987-88; *DyStar Textilfarben GmbH & Co. Deutschland KG*, 464 F.3d at

[5] The Examiner's finding of motivation is based in part on Rao's teaching that "double buffering provides concurrent update [of] one of the buffers and refresh from another buffer (see pages 5-9), which identifies and solves the same problem [as that of Appellant's system]" (Ans. 5, *see also* Final Office Action, mailed Nov. 29, 2006).

1360-61. Based on the arguments made in the Brief, we have no basis for questioning the findings of the Examiner. Appellant has not sustained his burden on appeal of showing that the Examiner erred in rejecting the claims on appeal as being unpatentable under 35 U.S.C. § 103(a).

Accordingly, we sustain the Examiner's rejection of claim 1. Appellant have not separately argued claims 2-3, 5-10, 12, 14-16, 18-20, 23-25, and 27-52. Therefore, we also sustain the Examiner's rejection of claims 2-3, 5-10, 12, 14-16, 18-20, 23-25, and 27-52.

DECISION

The decision of the Examiner is *affirmed*.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED

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